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(54) **Method of forming a polysilicon buried contact**

Verfahren zur Herstellung eines vergrabenen Kontaktes aus Polysilizium

Procédé de formation d'un contact enterré en silicium polycristallin

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Description

[0001] The present invention relates generally to semiconductor integrated circuit proc ssing, and mor specifically to a method of forming a polysilicon buried contact.

[0002] To create a transistor, a polysilicon layer is deposited on top of a thin oxide layer. To form a resistor, a polysilicon layer is deposited on a field oxide layer. Both of these semiconductor devices may be made from the same polysilicon layer during the same process steps. The polysilicon layer, however, must be electrically isolated from the silicon substrate in order for these devices to operate. A buried contact may also be made from the same polysilicon layer as the gate electrode of a transistor and a resistor. The buried contact, however, requires an electrical connection between the polysilicon layer and the silicon substrate, generally where polysilicon and diffusion wires interconnect.

[0003] In the case of the buried contact, an opening is made in the oxide layer overlying the silicon substrate to expose a portion of the silicon. If a split polysilicon layer, or two polysilicon layers, are used to form the gate electrodes and resistors, the second polysilicon layer may be used to form the buried contacts.

[0004] IBM Technical Disclosure Bulletin, Vol. 25, No. 8, January 1983, pp.4425-26 discloses a buried contact/ depletion device process which eliminates possible contamination of the gate silicon dioxide dielectric by the resist layer in the depletion device. This process incudes the steps recited in the pre-characterizing portion of claim 1 and provides a structure having the features of the pre-characterizing portion of claims 22 and 23.

[0005] Hewlett-Packard Journal, vol. 33, No. 10, pp. 21-27, 1982, discloses other method of forming buried contacts.

[0006] IBM Technical Disclosure Bulletin, Vol. 25, No. 8, January 1983, pp.4067-68 discloses a process for fabricating buried contacts in which palladium silicide is formed in the upper surface of the buried diffusion region so as to provide a contact having more uniform characteristics.

[0007] A split polysilicon process is generally used in SRAM applications. After the formation of a field oxide layer in the case of a resistor or diode, and a gate oxide layer in the case of a gate electrode, the first amorphous or polysilicon layer is deposited. The buried contact openings to the silicon substrate are patterned, etched and doped, if necessary. The second amorphous or polysilicon layer is then deposited, patterned and etched to form the upper portion of the split polysilicon of the gate electrodes and resistors as well as the buried contact in the contact opening which connects directly to the silicon substrate.

[0008] During the gate electrode and resistor split polysilicon etch, both amorphous silicon or polysilicon layers are etched over the gate oxide and field oxide regions. With the buried contact, however, since the second amorphous or polysilicon layer forms the contact, only the second layer is etched during the etch step since the first layer has been removed previously. The thickness of the second polysilicon layer is obviously less than the thickness of the total split polysilicon stack forming the gate electrodes or resistors from the first and s cond polysilicon layers. In other words, the distance to etch the second polysilicon layer from the top of the resistors to the substrate is substantially less than the distance to etch the layer from the top of the gate electrode or resistor to the gate oxide or the field oxide..

[0009] At the location of the buried contact, there is no natural etch stop at the surface of the substrate such as oxide. In order to completely dry etch the gate electrodes and resistors, an overetching situation occurs while etching the buried contact due to the lesser height of polysilicon over the buried contact in relation to the height of the gates and resistors. This overetching condition results in an undesirable trenching of the silicon substrate. The depth of the trench is a function of the relative thicknesses of the first and second split polysilicon layers, as well as the surface topography. These factors dictate the amount of overetch required to clear the polysilicon away from the edge of the active areas around the gate and resistor devices.

[0010] In order to prevent the trenches from forming in the substrate during the dry etch process of the second split polysilicon layer, the present invention uses an etch stop layer disposed over the silicon substrate. This additional layer will act as an etch stop in any subsequent polysilicon etch to prevent trenching the silicon substrate around the buried contact area. This layer will also improve the contact resistance between the buried contact and the substrate.

[0011] The invention may be incorporated into a method according to claim 1 for forming a semiconductor device structure, and the semiconductor device structure formed thereby, by forming a buried contact.

[0012] According to the present invention there is provided a. method of forming a buried contact of an integrated circuit comprising the steps of: forming an oxide layer on a substrate; forming a first silicon layer over the oxide layer; forming and patterning a first photoresist layer over the first silicon layer; etching the first silicon layer to form an opening therethrough which exposes a portion of the oxide layer; wherein an edge is formed in the first silicon layer; etching the oxide layer through the opening to expose a portion of the underlying substrate; depositing a conductive etch stop layer over the exposed portion of the substrate and the first photoresist layer; wherein the edge of the first silicon layer is covered by the conductive etch stop layer; removing the first photoresist layer and the portion of the etch stop layer disposed over the first photoresist layer; forming a second silicon layer over the first silicon layer and the remaining conductive etch stop layer; and etching the first and second silicon layers to expose a portion of the conductive etch stop layer and to form a conductive struc-

tur contacting th xposed portion of the substrate through the conductive etch stop layer.

[0013] The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mod of use, and further objects and advantages thereof, will best be understood by referenc to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

[0014] **Figures 1-4** and **6** are cross-sectional views of the fabrication of a semiconductor device structure according to the present invention.

[0015] **Figure 5** is a top plan view of a portion of a semiconductor device structure according to the present invention.

[0016] The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

[0017] Referring to **Figure 1**, an integrated circuit device is to be formed in a silicon substrate **10**. A field oxide layer **12** is formed over a portion of the substrate **10** by methods known in the art leaving an active region exposed. An oxide layer **14** is then formed over the exposed active region which is a portion of the substrate **10** not covered by the field oxide **12**. A first silicon layer 16 is deposited over the oxide layer **14** and the field oxide layer **12**. The first silicon layer may be amorphous silicon or polysilicon. Photoresist layer **18** is then formed and patterned, as known in the art, over the first silicon layer **16**.

[0018] Referring to **Figure 2**, the first silicon layer **16** is etched to form an opening **20** to expose a portion of the oxide layer **14**. The oxide layer **14** is then etched in the opening **20** to expose a portion of the substrate **10**. At this stage, the substrate **10** may be doped through opening **20** to form an active layer **22** which is oppositely doped from the underlying substrate **10**. Depending upon the nature of the doping material used, the dopant may also penetrate the amorphous or polysilicon layer **16** along each sidewall in opening **20**. Before any subsequent deposition steps, an in-situ predeposition cleaning of any native oxide may need to be performed.

[0019] A conductive etch stop layer **24**, such as a refractory metal silicide, is deposited over the first photoresist layer **18** and the exposed portion of substrate **10** in opening **20** by methods known in the art. The thickness of the etch stop layer will be typically between approximately 100 and 1000 angstroms (10 angstroms = 1 nm). The etch stop layer is deposited at a temperature which is low enough so that the first photoresist layer **18** does not flow or decompose. The actual temperatur for deposition of the conductive etch stop layer will depend upon the chemical structure of the photoresist.

[0020] Th conductive etch stop layer **24** may also be a refractory metal, refractory metal nitride or a composite layer such as a refractory metal/refractory metal nitride, refractory metal/refractory metal silicide or refractory metal nitride/refractory metal silicide. The conductive etch stop layer will act as an etch stop for subsequent etching processes as well as to reduce contact resistance. If a refractory metal or refractory metal nitride, for example, is used, the etch stop layer is annealed after the deposition process. Annealing, by rapid thermal annealing, will form a metal silicide in the interface between the substrate **10** and the conductive etch stop layer **24**. Any refractory metal or refractory metal nitride remaining after the anneal step may be removed to clean the surface of the etch stop layer.

[0021] Referring to **Figure 3**, the first photoresist layer **18** is removed using a lift-off process as known in the art. During the lift-off process, the first photoresist layer **18** and the portion of the etch stop layer **24** covering the first photoresist layer **18** are removed.

[0022] A second silicon layer **26** is next deposited over the first silicon layer **16** and the remaining conductive etch stop layer **24** by methods known in the art. Layer **26** may be comprised of amorphous silicon or polysilicon. A second photoresist layer **28** is formed and patterned over the second polysilicon layer **26** as known in the art. At this stage, the second polysilicon layer **26** may be selectively doped by known methods to achieve the doping level required for the various devices to be made from this layer.

[0023] Referring to **Figure 4**, the first and second silicon layers **16** and **26** are then etched to form a conductive structure which contacts the exposed portion of the substrate **10** through the conductive etch stop layer **24**. Lightly doped source/drain (LDD) regions **32** are formed in substrate **10**. Oxide sidewall spacers **34** are then formed on the sidewalls of the first and second silicon layers **16** and **26**. A heavily doped source/drain region **36** is then formed by methods known in the art. As will be shown by the plan view in **Figure 5**, the first and second silicon layers **16** and **26** form a resistor **38** and a gate **40**. Active layer **22** and the source/drain region **36** connect outside the plane of the drawing as will be shown in **Figure 5**.

[0024] Referring to **Figure 5**, the oxide layer **14** covers the substrate **10** not covered by the field oxide **12** except for the portion exposed in the opening **20**. The oxide sidewall spacers **34** surround the resistor **38** and the gate **40**. The conductive etch stop layer **24** is shown through the opening 20 and is continuous under resistor **38**. The etch stop layer **24** overlies the doped active layer **22** (shown in **Figure 4**) which connects to the source/drain region **36** underlying the oxide layer **14**.

[0025] **Figure 6** is a cross sectional view along the

line B-B as shown in the plan view of **Figur 5**. Opening **20** shows the etch stop layer **24** as filling the opening **20**. Source/drain regions **36** underli the oxid layer **14** except under the r sistor **38** and the gate **40** (not shown). The source/drain regions **36** and th active layer **22** are both formed in thos regions in the opening **20** not covered by th resistor **38**. This forms a continuous conductive region in the substrate **10**, allowing the resistor **38** to connect to the source/drain region **36** of the gate **40**.

[0026] As will be understood by those skilled in the art, oxide layer **14** protects the underlying substrate **10** during the etching of the gate **40** and resistor **38**. However, there is no oxide within the opening **20** to protect the underlying substrate. The etch stop layer **24** within the opening **20** protects the underlying substrate during the etch step which forms gate **40** and resistor **38**. The etch stop layer prevents trenching of the substrate **10** within the opening **20** which are not covered by the resistor **38**. As will be appreciated by those skilled in the art, prevention of such trenching improves the quality of the buried contact. In addition to preventing trenching, the conductive etch stop layer **24** reduces contact resistance as known in the art.

[0027] As will be appreciated by those skilled in the art, the process steps described above can be used with nearly any conventional process flow.

Claims

1. A method of forming a buried contact of an integrated circuit comprising the steps of:

   forming an oxide layer (14) on a substrate (10);
   forming a first silicon layer (16) over the oxide layer (14);
   forming and patterning a first photoresist layer (28) over the first silicon layer;
   etching the first silicon layer (16) to form an opening (20) therethrough which exposes a portion of the oxide layer; wherein an edge of said first silicon layer forms the sidewall of said opening ;
   etching the oxide layer through the opening to expose a portion of the underlying substrate (10);
   depositing a conductive etch stop layer (24) over the exposed portion of the substrate and the first photoresist layer (18); wherein the edge of the first silicon layer (16) is covered by the conductive etch stop layer;
   removing the first photoresist layer (18) and the portion of the etch stop layer (24) disposed over the first photoresist layer;
   forming a second silicon layer (26) over the first silicon layer (16) and the remaining conductive etch stop layer (24); and
   etching the first and second silicon layers (16,26) to expose a portion of the conductive etch stop layer within th opening (20) and to form a conductive structure contacting the exposed portion (10) of the substrate through the conductive etch stop layer (24).

2. A method as claimed in claim 1, comprising the step of forming a field oxide region (12) over a portion of the substrate (10) leaving an exposed active region, and wherein the oxide layer (14) is formed over the active region, and the first silicon layer (16) is formed over the oxide layer (14) and the field oxide region (12).

3. The method of claims 1 or 2, wherein each silicon layer is amorphous silicon.

4. The method of claim 1 or 2, wherein each silicon layer is polysilicon.

5. The method of any preceding claim, wherein the etch stop layer is a refractory metal silicide.

6. The method of any of claims 1 to 4, wherein the etch stop layer is a refractory metal nitride.

7. The method of claim 6, wherein the refractory metal nitride is annealed after the step of forming an etch stop layer to form a refractory metal silicide.

8. The method of claim 7, wherein the annealing step is performed by rapid thermal annealing.

9. The method of claim 7 or 8, wherein any refractory metal nitride remaining after the anneal step, is removed before the step of forming a silicon layer over the etch stop layer.

10. The method of any preceding claim, wherein the thickness of the etch stop layer is between approximately 10 and 100 nm (100 and 1000 angstroms).

11. The method of any preceding claim, further comprising the steps of:
    in-situ predeposition cleaning of a native oxide before the etch stop layer step.

12. The method of any preceding claim, further comprising the step of:
    cleaning the surface of the integrated circuit before the second silicon layer step.

13. The method of any preceding claim, further comprising the step of: selectively doping portions of the second silicon layer before etching the second silicon layer step.

14. The method of claim 2 or any of claims 3-13 when appended thereto, wherein the conductive structur extends to a resistor having a portion disposed over the field oxide region.

15. The method of any preceding claim, wherein th conductive etch stop layer is deposited at a temperature low enough so that the first photoresist layer does not flow or decompose.

16. The method of any preceding claim, further comprising the step of: doping the exposed portion of the substrate before forming an etch stop layer step.

17. The method of any preceding claim, comprising the step of selectively doping the second silicon layer before the etching of the second silicon layer.

18. The method as claimed in any preceding claim, wherein the first silicon layer and the etch stop layer overlying the first silicon layer are removed by a photoresist lift-off process.

19. A method as claimed in claim 2 or any one of the preceding claims when appended thereto, further comprising a gate disposed over the oxide layer.

Patentansprüche

1. Verfahren zur Ausbildung eines vergrabenen Kontaktes einer integrierten Schaltung, das die Schritte aufweist:

   eine Oxidschicht (14) wird auf einem Substrat (10) ausgebildet;
   eine erste Siliziumschicht (16) wird über der Oxidschicht (14) ausgebildet;
   eine erste Fotoresist- bzw. Fotolackschicht (28) wird über der ersten Siliziumschicht ausgebildet;
   die erste Siliziumschicht (16) wird geätzt, um eine Offnung (20) durch diese auszubilden, die einen Abschnitt der Oxidschicht freilegt; wobei eine Kante dieser ersten Siliziumschicht die Seitenwand der Öffnung bildet;
   die Oxidschicht wird durch die Öffnung geätzt, um einen Abschnitt des darunterliegenden Substrats freizulegen;
   eine leitende Ätzstoppschicht (24) wird über dem freigelegten Abschnitt des Substrats und der ersten Fotoresist- bzw. Fotolackschicht (18) abgeschieden; wobei die Kante der ersten Siliziumschicht (16) durch die leitende Ätzstoppschicht bedeckt ist;
   die erste Fotoresist- bzw. Fotolackschicht (18) und der Abschnitt der Ätzstoppschicht (24), der über der ersten Fotoresist- bzw. Fotolackschicht angeordnet ist, werden entfernt;
   eine zweite Siliziumschicht (26) wird über der ersten Siliziumschicht (16) und der verbleibenden leitenden Ätzstoppschicht (24) ausgebildet; und
   die erste und die zweit Siliziumschicht (16, 26) werden geätzt, um einen Abschnitt der leitenden Ätzstoppschicht innerhalb der Öffnung (20) freizulegen und um eine leitende Struktur zu bilden, die den freigelegten Abschnitt (10) des Substrats über die leitende Ätzstoppschicht (24) kontaktiert.

2. Verfahren nach Anspruch 1, das den Schritt aufweist, daß ein Feldoxidbereich (12) über einem Abschnitt des Substrats (10) ausgebildet wird, wobei ein freigelegter aktiver Bereich gelassen wird, und wobei die Oxidschicht (14) über dem aktiven Bereich ausgebildet wird, und die erste Siliziumschicht (16) über der Oxidschicht (14) und dem Feldoxidbereich (12) ausgebildet wird.

3. Verfahren nach Anspruch 1 oder 2, wobei jede Siliziumschicht aus amorphem Silizium ist.

4. Verfahren nach Anspruch 1 oder 2, wobei jede Siliziumschicht Polysilizium ist.

5. Verfahren nach einem der voranstehenden Ansprüche, wobei die Ätzstoppschicht ein hochbelastbares bzw. hochschmelzendes Metallsilizid ist.

6. Verfahren nach einem der Ansprüche 1 bis 4, wobei die Ätzstoppschicht ein hochbelastbares bzw. hochschmelzendes Metallnitrid ist.

7. Verfahren nach Anspruch 6, wobei das hochbelastbare bzw. hochschmelzende Metallnitrid nach dem Schritt zur Ausbildung einer Ätzstoppschicht geglüht bzw. getempert wird, um ein hochbelastbares bzw. hochschmelzendes Metallsilizid zu bilden.

8. Verfahren nach Anspruch 7, wobei der Temperungs- bzw. Glühschritt durch schnelles thermisches Tempern bzw. Glühen durchgeführt wird.

9. Verfahren nach einem der Ansprüche 7 oder 8, wobei irgendein hochschmelzendes bzw. hochbelastbares Metallnitrid, das nach dem Glüh- bzw. Temperungsschritt zurückbleibt, vor dem Schritt zur Ausbildung einer Siliziumschicht über der Ätzstoppschicht entfernt wird.

10. Verfahren nach einem der voranstehenden Ansprüche, wobei die Dicke der Ätzstoppschicht zwischen näherungsweise 10 und 100 nm (100 bis 1000 Angström) liegt.

11. Verfahren nach einem der voranstehenden Ansprüche, das ferner die Schritte aufweist:
eine in-situ-Vorabscheidungsreinigung eines ursprünglichen Oxids vor dem Schritt für die Ätzstoppschicht.

12. Verfahren nach einem der voranstehenden Ansprüche, das ferner den Schritt aufweist:
die Oberfläche der integrierten Schaltung wird vor dem Schritt für die zweite Siliziumschicht gereinigt.

13. Verfahren nach einem der voranstehenden Ansprüche, das ferner den Schritt aufweist: Abschnitt der zweiten Siliziumschicht werden vor dem Ätzen des zweiten Siliziumschichtschrittes selektiv dotiert.

14. Verfahren nach Anspruch 2 oder einem der Ansprüche 3 bis 13, wenn sie von diesen abhängen, wobei sich die leitende Struktur zu einem Widerstand erstreckt, der einen Abschnitt aufweist, der über dem Feldoxidbereich angeordnet ist.

15. Verfahren nach einem der voranstehenden Ansprüche, wobei die leitende Ätzstoppschicht bei einer Temperatur abgelagert wird, die niedrig genug ist, so daß die erste Fotoresistschicht nicht fließt oder sich zersetzt.

16. Verfahren nach einem der voranstehenden Ansprüche, das ferner den Schritt aufweist: der abgeschiedene Abschnitt des Substrats wird dotiert, bevor ein Ätzstoppschichtschritt gebildet wird.

17. Verfahren nach einem der voranstehenden Ansprüche, das den Schritt aufweist, daß die zweite Siliziumschicht selektiv vor dem Ätzen der zweiten Siliziumschicht dotiert wird.

18. Verfahren nach einem der voranstehenden Ansprüche, wobei die erste Siliziumschicht und die Ätzstoppschicht, die die erste Siliziumschicht überdeckt, durch einen Fotoresist- bzw. Fotolackabhebeprozeß entfernt werden.

19. Verfahren nach Anspruch 2 oder nach einem der voranstehenden Ansprüche, wenn diese von diesen abhängen, das ferner ein Gate aufweist, das über der Oxidschicht angeordnet ist.

Revendications

1. Procédé de formation d'un contact enterré dans un circuit intégré comprenant les étapes suivantes :

former une couche d'oxyde (14) sur un substrat (10) ;
former une première couche de silicium (16) sur la couche d'oxyde (14) ;
former et graver une première couche de produit photosensible (28) sur la première couche de silicium ;
graver la première couche de silicium (16) pour former une ouverture (20) au travers et exposer une partie de la couche d'oxyde ; un bord de la première couche de silicium formant la paroi latérale de l'ouverture ;
graver la couche d'oxyde à travers l'ouverture pour exposer une partie du substrat sous-jacent (10) ;
déposer une couche d'arrêt de gravure conductrice (24) sur la partie exposée du substrat et la première couche de produit photosensible (18), le bord de la première couche de silicium (16) étant couvert de la couche d'arrêt de gravure conductrice ;
enlever la première couche de produit photosensible (18) et la partie de la couche d'arrêt de gravure (24) déposée sur la première couche de produit photosensible ;
former une seconde couche d'oxyde (26) sur la première couche de silicium (16) et la couche d'arrêt de gravure conductrice restante (24) ; et graver les première et seconde couches de silicium (16, 26) pour exposer une partie de la couche d'arrêt de gravure conductrice à l'intérieur de l'ouverture (20) et pour former une structure conductrice contactant la partie exposée (10) du substrat à travers la couche d'arrêt de gravure conductrice (24).

2. Procédé selon la revendication 1, comprenant l'étape consistant à former une région d'oxyde de champ (12) sur une partie du substrat (10) laissant une région active exposée, et dans lequel la couche d'oxyde (14) est formée sur la région active, et la première couche de silicium (16) est formée sur la couche d'oxyde (14) et la région d'oxyde de champ (12).

3. Procédé selon la revendication 1 ou 2, dans lequel chaque couche de silicium est en silicium amorphe.

4. Procédé selon la revendication 1 ou 2, dans lequel chaque couche de silicium est en silicium polycristallin.

5. Procédé selon l'une quelconque des revendications précédentes, dans lequel la couche d'arrêt de gravure est en siliciure de métal réfractaire.

6. Procédé selon l'une quelconque des revendications 1 à 4, dans lequel la couche d'arrêt de gravure est en nitrure de métal réfractaire.

7. Procédé selon la revendication 6, dans lequel le nitrur de métal réfractaire est recuit après l'étape de formation d'une couche d'arrêt de gravur pour former un siliciure de métal réfractaire.

8. Procédé selon la revendication 7, dans lequel l'étape de recuit est réalisée par recuit th rmique rapide.

9. Procédé selon la revendication 7 ou 8, dans lequel tout nitrure de métal réfractaire restant en place après l'étape de recuit est éliminé avant l'étape de formation d'une couche de silicium sur la couche d'arrêt de gravure.

10. Procédé selon l'une quelconque des revendications précédentes, dans lequel l'épaisseur de la couche d'arrêt de gravure est comprise entre environ 10 et 100 nm (100 et 1000 angströms).

11. Procédé selon l'une quelconque des revendications précédentes, comprenant en outre l'étape consistant à nettoyer in situ un prédépôt d'un oxyde natif avant l'étape de formation de la couche d'arrêt de gravure.

12. Procédé selon l'une quelconque des revendications précédentes, comprenant en outre l'étape consistant à nettoyer la surface du circuit intégré avant l'étape de formation de la seconde couche de silicium.

13. Procédé selon l'une quelconque des revendications précédentes, comprenant en outre l'étape consistant à doper sélectivement des parties de la seconde couche de silicium avant de graver la seconde couche de silicium.

14. Procédé selon la revendication 2 ou l'une quelconque des revendications 3 à 13 prises dans la dépendance de cette revendication, dans lequel la structure conductrice s'étend à une résistance comportant une partie déposée au-dessus de la région d'oxyde de champ.

15. Procédé selon l'une quelconque des revendications précédentes, dans lequel la couche d'arrêt de gravure conductrice est déposée à une température suffisamment basse pour que la première couche de produit photosensible ne flue ni ne se décompose.

16. Procédé selon l'une quelconque des revendications précédentes, comprenant les étapes consistant à doper la partie exposée du substrat avant de former une couche d'arrêt de gravure.

17. Procédé selon l'une quelconque des revendications précédentes, comprenant l'étape consistant à doper sélectivement la second couche d silicium avant la gravure de la seconde couche de silicium.

18. Procédé selon l'une quelconque des revendications précédentes, dans lequel la premièr couche de silicium et la couche d'arrêt de gravur recouvrant la premièr couche de silicium sont enlevées par un procédé de soulèvement de produit photosensible.

19. Procédé selon la revendication 2, ou l'une quelconque des revendications qui en dépendent, comprenant en outre une grille disposée au-dessus de la couche d'oxyde.

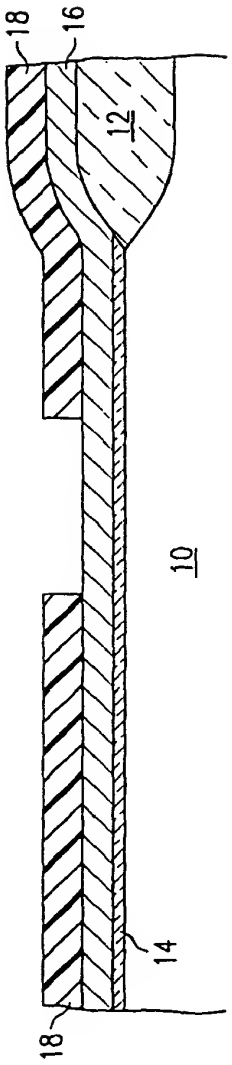

FIG. 1

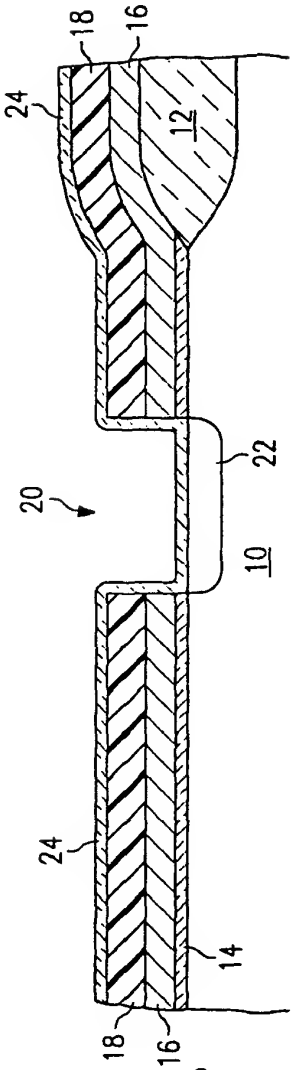

FIG. 2

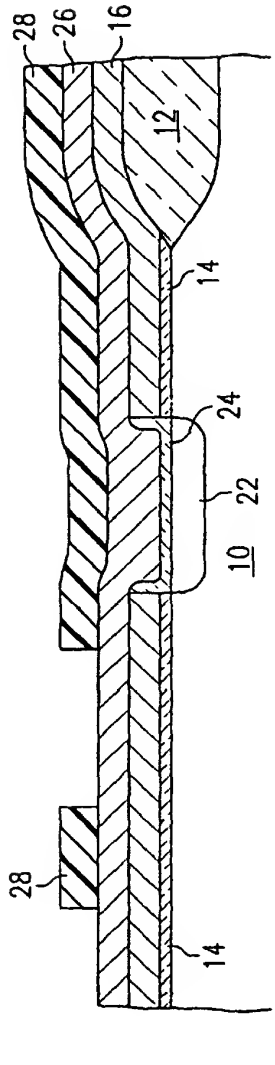

FIG. 3

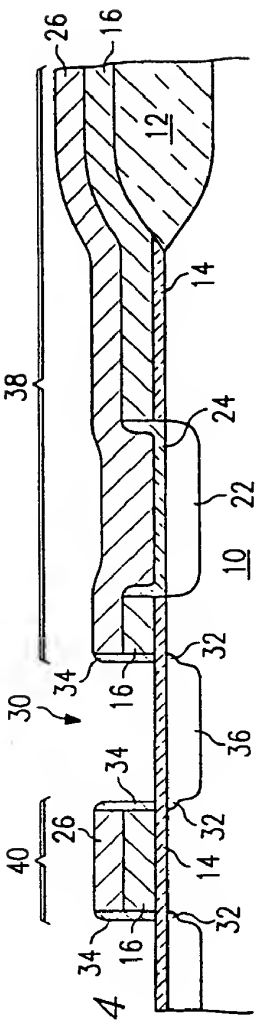

FIG. 4

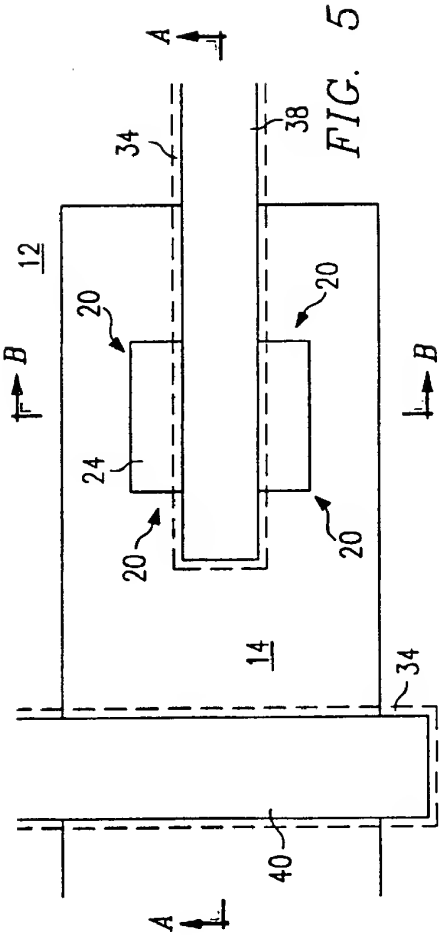

FIG. 5

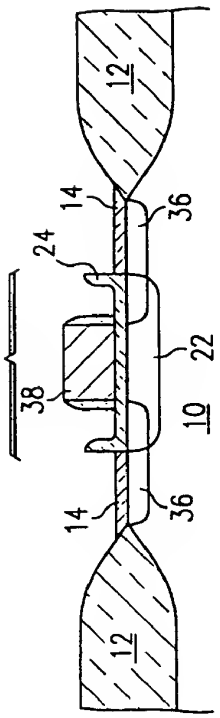

FIG. 6

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(54) Method of forming a polysilicon buried contact.

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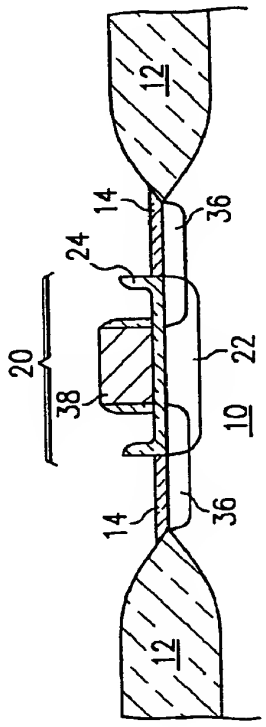

FIG. 6

EP 0 526 244 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 30 7018

PAGE1

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 25, no. 8, January 1983, NEW YORK US pages 4425 - 4426 R. C. DOCKERTY * the whole document *	1,3,4,14	H01L21/74
Y	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 25, no. 8, January 1983, NEW YORK US pages 4067 - 4068 A. EDENFELD ET AL * the whole document *	1,3,6,14	
Y	HEWLETT-PACKARD JOURNAL vol. 33, no. 10, October 1982, AMSTELVEEN NL pages 21 - 27 HORNG-SEN FU ET AL * page 25; figures 1,2 *	4,6	
A	IBM TECHNICAL DISCLOSURE BULLETIN. vol. 24, no. 7B, December 1981, NEW YORK US pages 3696 - 3697 G. J. HU ET AL * the whole document *	1,6,10, 13-17	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01L
A	EP-A-0 209 794 (FUJITSU LIMITED) * page 4, line 31 - page 7, line 29; figures 3A-3D *	1,3,6,16	
A	US-A-4 413 402 (D. M. ERB) * column 3, line 20 - column 5, line 15 *	1,6,16	
A	US-A-4 033 026 (R. D. PASHLEY) * column 4, line 1 - line 57 *	1	
A	US-A-4 657 628 (T. C. HOLLOWAY ET AL) * abstract *	7,12	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	25 MAY 1993	ROUSSEL A.T.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 30 7018
PAGE2

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4 187 602 (D. J. MC ELROY) * column 4, line 29 - column 5, line 31; figure 4 *	12	
A	PHILIPS JOURNAL OF RESEARCH vol. 44, no. 2/3, 28 July 1989, EINDHOVEN NL pages 257 - 291 K. OSINSKI ET AL * paragraph 3.1 *	8,17	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

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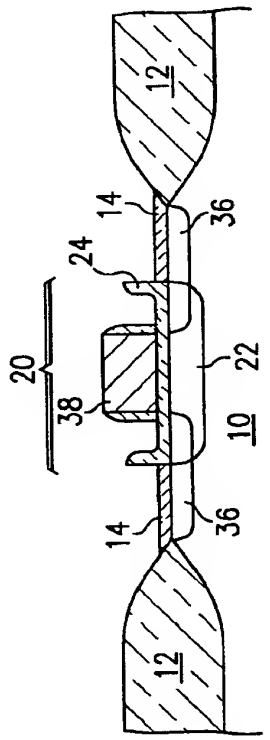


FIG. 6

EP 0 526 244 A2

Th present invention relates generally to semiconductor integrated circuit processing, and mor sp cifically to forming a p lysilicon buried contact.

To creat a transistor, a polysilicon layer is d posited on top of a thin oxide layer. To form a resistor, a polysilicon layer is deposited on a fi ld oxide lay r. Both of these semiconductor devices may be made from the same polysilicon layer during the same process steps. The polysilicon layer, however, must be electrically isolated from the silicon substrate in order for these devices to operate. A buried contact may also be made from the same polysilicon layer as the gate electrode of a transistor and a resistor. The buried contact, however, requires an electrical connection between the polysilicon layer and the silicon substrate, generally where polysilicon and diffusion wires interconnect.

In the case of the buried contact, an opening is made in the oxide layer overlying the silicon substrate to expose a portion of the silicon. If a split polysilicon layer, or two polysilicon layers, are used to form the gate electrodes and resistors, the second polysilicon layer may be used to form the buried contacts.

The split polysilicon process is generally used in SRAM applications. After the formation of a field oxide layer in the case of a resistor or diode, and a gate oxide layer in the case of a gate electrode, the first amorphous or polysilicon layer is deposited. The buried contact openings to the silicon substrate are patterned, etched and doped, if necessary. The second amorphous or polysilicon layer is then deposited, patterned and etched to form the upper portion of the split polysilicon of the gate electrodes and resistors as well as the buried contact in the contact opening which connects directly to the silicon substrate.

During the gate electrode and resistor split polysilicon etch, both amorphous silicon or polysilicon layers are etched over the gate oxide and field oxide regions. With the buried contact, however, since the second amorphous or polysilicon layer forms the contact, only the second layer is etched during the etch step since the first layer has been removed previously. The thickness of the second polysilicon layer is obviously less than the thickness of the total split polysilicon stack forming the gate electrodes or resistors from the first and second polysilicon layers. In other words, the distance to etch the second polysilicon layer from the top of the resistors to the substrate is substantially less than the distance to etch the layer from the top of the gate electrode or resistor to the gate oxide or the field oxide..

At the location of the buried contact, there is no natural etch stop at the surface of the substrate such as oxide. In order to completely dry etch the gate electrodes and resistors, an overetching situation occurs while etching the buried contact due to the lesser height of polysilicon over the buried contact in r lation to th h ight of the gates and resistors. This ov retching condition results in an undesirabl trenching of th silicon substrat . The depth of th tr nch is a function of the relative thickness s f the first and second split polysilicon layers, as w ll as the surface top graphy. These factors dictate the amount of overetch required to clear the polysilic n away from th edg of the active areas around the gate and resistor devices.

In order to prevent the trenches from forming In the substrate during the dry etch process of the second split polysilicon layer, the present invention uses an etch stop layer disposed over the silicon substrate. This additional layer will act as an etch stop in any subsequent polysilicon etch to prevent trenching the silicon substrate around the buried contact area. This layer will also improve the contact resistance between the buried contact and the substrate.

The invention may be incorporated into a method for forming a semiconductor device structure, and the semiconductor device structure formed thereby, by forming a buried contact. To form the buried contact, an oxide layer is formed over a substrate. A first silicon layer may be formed over the oxide layer at this stage. An opening through the first silicon layer and the oxide layer is formed exposing a portion of the underlying substrate. A conductive etch stop layer is then formed over the exposed substrate. A second silicon layer is formed over the first silicon layer and the etch stop layer. A portion of the first and second silicon layers is then etched to form a conductive structure contacting the exposed portion of the substrate through the etch stop layer.

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein:

Figures 1-4 and **6** are cross-sectional views of the fabrication of a semiconductor device structure according to the present invention.

Figure 5 is a top plan view of a portion of a semiconductor device structure according to the present invention.

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

Referring to **Figur 1**, an integrated circuit device

is to be formed in a silicon substrate **10**. A field oxide layer **12** is formed over a portion of the substrate **10** by methods known in the art leaving an active region exposed. An oxide layer **14** is then formed over the exposed active region which is a portion of the substrate **10** not covered by the field oxide **12**. A first silicon layer **18** is deposited over the oxide layer **14** and the field oxide layer **12**. The first silicon layer may be amorphous silicon or polysilicon. Photoresist layer **18** is then formed and patterned, as known in the art, over the first silicon layer **16**.

Referring to **Figure 2**, the first silicon layer **16** is etched to form an opening **20** to expose a portion of the oxide layer **14**. The oxide layer **14** is then etched in the opening **20** to expose a portion of the substrate **10**. At this stage, the substrate **10** may be doped through opening **20** to form an active layer **22** which is oppositely doped from the underlying substrate **10**. Depending upon the nature of the doping material used, the dopant may also penetrate the amorphous or polysilicon layer **16** along each sidewall in opening **20**. Before any subsequent deposition steps, an in-situ predeposition cleaning of any native oxide may need to be performed.

A conductive etch stop layer **24**, such as a refractory metal silicide, is deposited over the first photoresist layer **18** and the exposed portion of substrate **10** in opening **20** by methods known in the art. The thickness of the etch stop layer will be typically between approximately 100 and 1000 angstroms. The etch stop layer is deposited at a temperature which is low enough so that the first photoresist layer **18** does not flow or decompose. The actual temperature for deposition of the conductive etch stop layer will depend upon the chemical structure of the photoresist.

The conductive etch stop layer **24** may also be a refractory metal, refractory metal nitride or a composite layer such as a refractory metal/refractory metal nitride, refractory metal/refractory metal silicide or refractory metal nitride/refractory metal silicide. The conductive etch stop layer will act as an etch stop for subsequent etching processes as well as to reduce contact resistance. If a refractory metal or refractory metal nitride, for example, is used, the etch stop layer is annealed after the deposition process. Annealing, by rapid thermal annealing, will form a metal silicide in the interface between the substrate **10** and the conductive etch stop layer **24**. Any refractory metal or refractory metal nitride remaining after the anneal step may be removed to clean the surface of the etch stop layer.

Referring to **Figure 3**, the first photoresist layer **18** is removed using a lift-off process as known in the art. During the lift-off process, the first photoresist layer **18** and the portion of the etch stop layer **24** covering the first photoresist layer **18** are removed.

A second silicon layer **26** is next deposited over the first silicon layer **16** and the remaining conductive etch stop layer **24** by methods known in the art. Layer **26** may be comprised of amorphous silicon or polysilicon. A second photoresist layer **28** is formed and patterned over the second polysilicon layer **26** as known in the art. At this stage, the second polysilicon layer **26** may be selectively doped by known methods to achieve the doping level required for the various devices to be made from this layer.

Referring to **Figure 4**, the first and second silicon layers **16** and **26** are then etched to form a conductive structure which contacts the exposed portion of the substrate **10** through the conductive etch stop layer **24**. Lightly doped source/drain (LDD) regions **32** are formed in substrate **10**. Oxide sidewall spacers **34** are then formed on the sidewalls of the first and second silicon layers **16** and **26**. A heavily doped source/drain region **36** is then formed by methods known in the art. As will be shown by the plan view in **Figure 5**, the first and second silicon layers **16** and **26** form a resistor **38** and a gate **40**. Active layer **22** and the source/drain region **36** connect outside the plane of the drawing as will be shown in **Figure 5**.

Referring to **Figure 5**, the oxide layer **14** covers the substrate **10** not covered by the field oxide **12** except for the portion exposed in the opening **20**. The oxide sidewall spacers **34** surround the resistor **38** and the gate **40**. The conductive etch stop layer **24** is shown through the opening 20 and is continuous under resistor **38**. The etch stop layer **24** overlies the doped active layer **22** (shown in **Figure 4**) which connects to the source/drain region **36** underlying the oxide layer **14**.

Figure 6 is a cross sectional view along the line B-B as shown in the plan view of **Figure 5**. Opening **20** shows the etch stop layer **24** as filling the opening **20**. Source/drain regions **36** underlie the oxide layer **14** except under the resistor **38** and the gate **40** (not shown). The source/drain regions **36** and the active layer **22** are both formed in those regions in the opening **20** not covered by the resistor **38**. This forms a continuous conductive region in the substrate **10**, allowing the resistor **38** to connect to the source/drain region **36** of the gate **40**.

As will be understood by those skilled in the art, oxide layer **14** protects the underlying substrate **10** during the etching of the gate **40** and resistor **38**. However, there is no oxide within the opening **20** to protect the underlying substrate. The etch stop layer **24** within the opening **20** protects the underlying substrate during the etch step which forms gate **40** and resistor **38**. The etch stop layer prevents trenching of the substrate **10** within the opening **20** which are not covered by the resistor **38**. As will be appreciated by those skilled in the art, prevention of such trenching improves the quality of the buried contact. In addition to preventing trenching, the conductive etch stop layer **24** reduces contact resistance as known in the art.

As an alternative to the above described two lay-

er polysilicon resistor and gat , a single polysilicon layer may be used. In such a process, the first polysilicon layer **16** is omitted. All ther process steps ar performed as described abov .

As will be appreciated by those skilled in the art, the process steps described above can b used with nearly any conventional process flow. While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

Claims

1. A method of forming a buried contact of an integrated circuit comprising the steps of:
   forming an oxide layer over a substrate;
   forming an opening through the oxide layer to expose a portion of the underlying substrate;
   forming a conductive etch stop layer over the exposed substrate;
   forming a first silicon layer over the etch stop layer; and,
   etching a portion of the first silicon layer to form a conductive structure contacting the exposed portion of the substrate through the etch stop layer.

2. The method of Claim 1, wherein the thickness of the etch stop layer is between approximately 100 and 1000 angstroms.

3. The method of Claim 1, further comprising the step of: in-situ predeposition cleaning of a native oxide before the forming an etch stop layer step.

4. The method of Claim 1, further comprising the step of: forming a second silicon layer over the oxide layer before the forming the opening step.

5. The method of Claim 4, further comprising the step of: cleaning the surface of the integrated circuit before the forming a second silicon layer step.

6. A method of forming a buried contact of an integrated circuit comprising the steps of:
   forming a field oxide region over a portion of a substrate leaving an exposed active region;
   forming an oxide layer over the active region;
   forming a first silicon layer over the oxide layer and the field oxide region;
   f rming and patterning a first photoresist lay r ov r th first silicon lay r;
   tching the first silicon lay r to form an opening therethrough xposing a portion of the oxide layer;
   tching the xide lay r through the opening exposing a porti n of th substrat ;
   forming a conductive etch stop layer over the exposed portion of the substrate and the first photoresist layer;
   removing the first photoresist layer and the etch stop layer disposed over the first photoresist layer;
   forming a second silicon layer over the first silicon layer and the remaining etch stop layer;
   forming and patterning a second photoresist layer over the second silicon layer; and,
   etching the first and second silicon layers to form a conductive structure contacting the exposed portion of the substrate through the etch stop layer.

7. The method of Claim 1 or 6, wherein the etch stop layer is a refractory metal nitride.

8. The method of Claim 7, wherein the refractory metal nitride is annealed after the step of forming an etch stop layer to form a refractory metal silicide.

9. The method of Claim 8, wherein the annealing step is performed by rapid thermal annealing.

10. The method of Claim 8, wherein any refractory metal nitride remaining after the anneal step, is removed before the step of forming a silicon layer over the etch stop layer.

11. The method of Claim 6, further comprising the step of: selectively doping portions of the second silicon layer before etching the second silicon layer step.

12. The method of Claim 6, wherein the first conductive structure is a gate electrode disposed over a gate oxide layer and the second conductive structure is a resistor disposed over a field oxide layer.

13. The method of Claim 6, wherein the first silicon layer and the etch stop layer overlying the first silicon layer are removed by a photoresist lift-off process.

14. The method of Claim 6, further comprising the step of: doping the exposed portion of the substrate before forming an etch stop layer step.

15. The method of Claim 6, wherein the conductive etch stop layer is deposited at a temperature low enough so that the first ph toresist layer do s not

flow r decompose.

16. A structure consisting of a portion of a semiconductor integrated circuit, comprising:
a substrat ;
a conductive etch stop lay r disposed ov r a portion of the substrate; and,
a conductive silicon element overlying the substrate, said element having a first layer overlying a portion of the substrate other than the conductive etch stop layer, and having a second layer overlying the first layer and overlying a portion of the conductive etch stop layer.

17. The method of Claim 1 or 6, or the structure of Claim 15, wherein the etch stop layer is a refractory metal silicide.

18. The method of Claim 1 or 6, or the structure of Claim 16, wherein each silicon layer is amorphous silicon.

19. The method of Claim 1 or 6, or the structure of Claim 16, wherein each silicon layer is polysilicon.

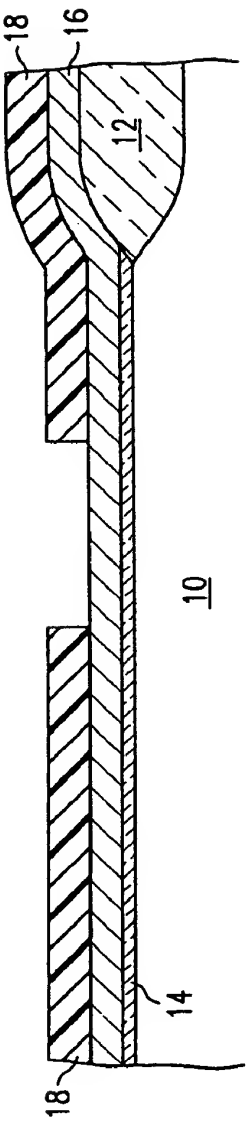


FIG. 1

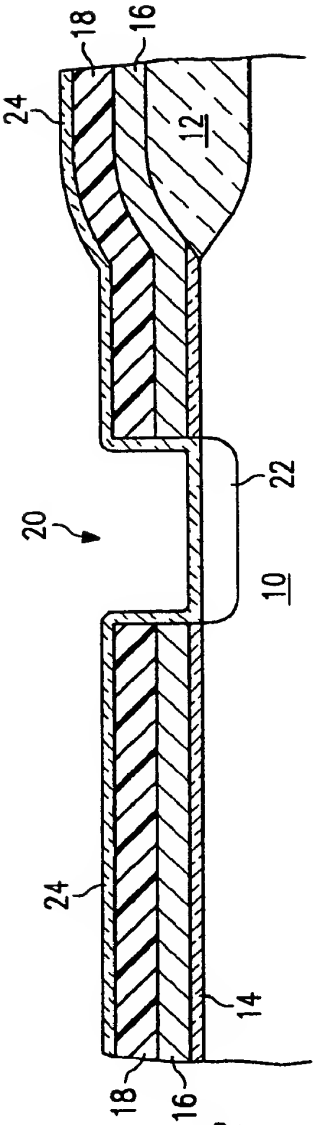


FIG. 2

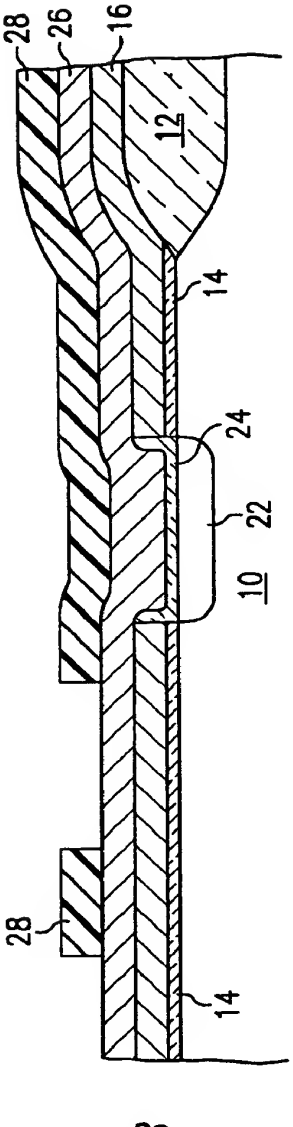


FIG. 3

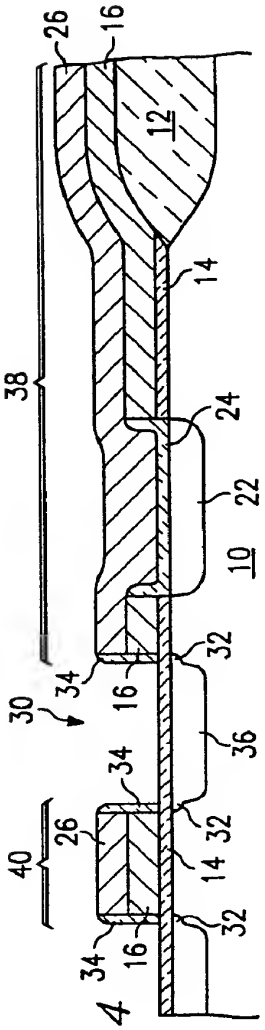
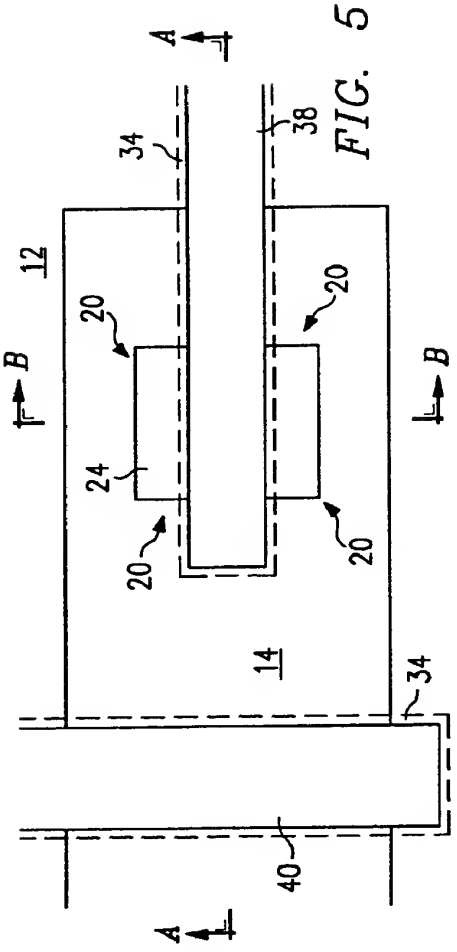


FIG. 4



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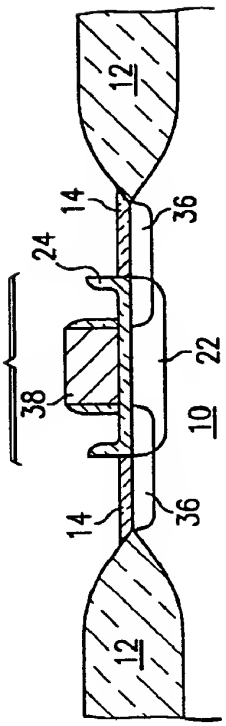

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